# MEMORY ACCESS CONTROL APPARATUS

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a memory interface, and more particularly, to a memory access control apparatus capable of writing image data in an external memory or reading the image data.

### 2. Description of the Conventional Art

Various image display apparatuses which are recently being developed need to non-linearly format-convert image data, that is not only in a horizontal direction but also in a vertical direction. As an application of the format-conversion, there are a pincushion method, a keystone method, and etc., which can be applied to various display apparatuses.

For example, in an image display apparatus such as a projector for projecting an image on a screen, when an image is displayed on a screen, a phenomenon that an image displayed on the screen is non-linearly distorted by the screen or by an optical mechanism limit is generated. Also, in an image display apparatus based on a general brown tube, an image distortion is not generated at the center of the brown tube by a screen of a curved surface but an image distortion is generated in an edge direction of the brown tube. According to this, the image display apparatus reverse-converts the distorted image into the

original image in an additional format conversion process block for compensating a partial distortion of the image. According to this, an actual image displayed on the screen is normally realized without a distortion, so that the user can see an image with an optimum state.

The image display apparatus outputs image data non-linearly when an image is to be displayed on the screen thus to display the original image on the screen without a distortion. Functions for non-linearly processing image data include a tilt function, a pincushion function, a keystone function, and etc., which is called as a warping function. In order to implement the warping function, the image data has to be accessed to an external memory in a vertical direction or a horizontal direction.

However, in the conventional memory access control apparatus, the warping function is performed by storing the image data in an external memory in a horizontal direction by a raster scan method and then reading the stored image data in a horizontal direction. Therefore, in the conventional memory access control apparatus, a memory access latency becomes very great thus not to be able to smoothly read image data from the external memory, thereby lowering a stability of the entire system. Hereinafter, a process for storing image data in the external memory in accordance with the conventional art will be explained with reference to Figure 1.

Figure 1 is a view for explaining a storage principle of image data in a memory access control apparatus in accordance with the conventional art.

As shown, the conventional memory access control apparatus stores inputted image data by sequentially increasing a column address inside the external memory. That is, since the conventional memory access control

apparatus consecutively processes the image data as an image line unit, a bank change of the external memory is not generated when the image data stored in the external memory is to be accessed in a horizontal direction of an image frame. According to this, the image data can be processed with a minimum memory access latency.

In the conventional memory access control apparatus, since a minimum memory access latency is used when adjacent image data stored in the external memory are accessed, a function of the entire system can be enhanced. Herein, the memory access latency is a delay time generated when image data stored in different banks and rows of the external memory are accessed, and can be represented as the number of memory operation clocks.

However, in the conventional memory access control apparatus, a considerable memory access latency is generated when image data sequentially stored in the external memory is read in a vertical direction of the image frame.

For example, when an interlaced scanning image of 512k x 64-bit x 4 banks SDRAM is accessed, 8 pixel data, that is, 8 bytes are stored in one column in the conventional memory access control apparatus. Therefore, in order to store one image line inside one image frame in the SDRAM, 240 (1920/8) columns are necessary. Generally, the $N^{th}$ bank of the $N^{th}$ row inside a memory has 256 columns, so that said one image line can be stored in the $N^{th}$ bank of the $N^{th}$ row inside the memory. Herein, said 8 pixel data is defined as one word.

In the conventional memory access control apparatus, when the memory where the image data is stored as 32 words is accessed, a bank change is performed at each image line in order to bring the stored image data in a vertical direction of the stored image frame. In a process for sending a command for the

bank change request to the SDRAM interface, a certain number of memory access latencies (for example, 6 clocks) are generated. That is, if the number of clocks necessary to access one word is 1, 32 clocks are required to bring 32 word data. Nevertheless, the number of clocks of the memory access latency generated during the bank change of 32 times is 191 (6 (the number of clocks) x 32 times –1 (the number of clocks)). According to this, in the conventional memory access control apparatus, a memory access efficiency of the entire system is greatly degraded, so that a high efficiency of a memory access of the entire system can not be ensured with the existing method.

As aforementioned, in the conventional memory access control apparatus, image data constituting one image frame is sequentially stored in the external memory by one-dimensional array method, so that the memory access latency for accessing image data of various display apparatuses in a vertical direction is increased.

## SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a memory access control apparatus capable of optimally controlling a memory access latency for various display apparatuses by calculating a bank, a row, and a column of a memory where image data is to be stored based on a coordinate value of image data constituting one image frame and predetermined data.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, there is provided a memory access control apparatus comprising: a memory

access control unit for storing image data in a memory by a two-dimensional array according to values of a bank, a row, and a column of the memory where the image data is to be stored calculated on the basis of coordinate values of the image data constituting one image frame and predetermined data.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

Figure 1 is a view for explaining a storage principle of image data in a memory access control apparatus in accordance with the conventional art;

Figure 2 is a view for explaining a storage principle of image data in a memory access control apparatus according to the present invention;

Figures 3A and 3B are views showing a memory structure where image data of Y and C components are arranged;

Figure 4 is a view showing a memory structure where image data of R, G, and B components are arranged;

Figure 5 is a view for explaining a principle for arranging image data of R,

G, and B components of Figure 4 in an SDRAM;

Figure 6 is a view for obtaining a physical address for storing image data according to the present invention; and

Figure 7 is a view showing a schematic construction of the memory access control apparatus according to the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Hereinafter, will be explained a memory access control apparatus capable of optimally controlling a memory access latency for various display apparatuses by calculating a bank, a row, and a column of a memory where image data is to be stored based on a coordinate value of image data constituting one image frame and predetermined data.

Figure 2 is a view for explaining a storage principle of image data in a memory access control apparatus according to the present invention.

As shown, in the memory access control apparatus according to the present invention, image data constituting one image frame is stored in the $N^{th}$ bank of the $N^{th}$ row in an external memory by a two-dimensional array method, so that the image data stored in the external memory can be accessed in a horizontal direction or a vertical direction with an optimum memory access latency.

A principle for storing the image data of the memory access control apparatus according to the present invention will be explained as follows.

The inputted image data is divided into image lines respectively

constituted with 256 words by regarding 8 bytes as one word. The image data of each image line is stored in a predetermined position of the external memory as a word unit.

Herein, the number of words that can be stored in one line in the $N^{th}$ bank of the $N^{th}$ row inside the memory is defined a word per bank, and the number of lines that can be included in the $N^{th}$ bank of the $N^{th}$ row inside the memory is defined as a unit line.

For example, in the external memory for storing the image data, first image data of 8 bytes of the image lines is sequentially stored in the first column in the $N^{th}$ bank of the $N^{th}$ row in a vertical direction, and second image data of 8 bytes of the image lines is sequentially stored in the second column in a vertical direction. By repeating said process, 960 pixels, a half of 1920 pixels of said each image line having the word per bank of 32 and the unit line of 8 are stored in the 0, 1, 2, and $3^{th}$ banks of the $0^{th}$ row inside the external memory. Also, the rest 960 pixels, a half of 1920 pixels of said each image line having the word per bank of 32 and the unit line of 8 are stored in the 0, 1, 2, and $3^{th}$ banks of the $1^{th}$ row inside the external memory.

In the memory access control apparatus according to the present invention, image data constituting one image frame is stored in the $N^{th}$ bank of the $N^{th}$ row inside the external memory by a two-dimensional array method. According to this, in case of accessing image data in a vertical direction or in a horizontal direction, the image data can be accessed with an optimum memory access latency.

Figures 3A and 3B are views showing a memory structure where image data of Y and C components are arranged.

As shown, 8 bytes including a luminance Y and a chrominance C of an image, that is, one word unit is stored in the memory structure. Herein, Figure 3A shows an array method for accessing image data of the Y and C components in one bank in one row, and Figure 3B shows an array method for accessing image data of the Y and C components in a bank of different rows.

Figure 4 is a view showing a memory structure where image data of R, G, and B components are arranged.

As shown, 8 bytes including R, G, and B components, that is, one word unit is stored in the memory structure. In case that image data of the R, G, and B components is stored in the memory structure, a garbage region that is not used may be generated in the $N^{th}$ bank of the $N^{th}$ row. However, said problem can be solved by consecutively arranging image data of the R, G, and B components.

Figure 5 is a view for explaining a principle for arranging image data of the R, G, and B components of Figure 4 in a synchronous dynamic random access memory (SDRAM).

Referring to Figure 5, in a 1920 x 1080 interlaced scanning image, image data stored in the SDRAM are stored in one unit line in one bank with 32 words, and one word is constituted with 8 pixels. Therefore, the number of rows necessary to store said one unit line in the memory is calculated as the following formula 1. The number of rows necessary to store said one unit line in the memory is defined as a row per unit line.

[Formula 1]

Row per unit line = 1.875 row = 1920 pixels / {8 (pixel/word) x 32 (word/bank) x 4 (bank/row)}

The number of rows occupied by one image frame in the external memory

is defined as an offset, and the offset is obtained as the following formula 2.

[Formula 2]

Offset = (vertical line/unit line) x row per unit line = (540/8) x 2 (rounding off) = 135 rows (rounding off)

Herein, the vertical line denotes the number of lines inside the memory where said one image frame is stored.

Figure 6 is a view for explaining an operation principle of the memory access control apparatus according to the present invention.

As shown, the memory access control apparatus according to the present invention comprises: a format conversion unit 10 for converting image data into a corresponding format for performing a warping function; a control unit 21 for storing the image data in a memory by a two-dimensional array method according to values of a row, a bank, and a column inside the memory where the image data is to be stored calculated on the basis of coordinate values of the converted image data and predetermined data; and a storing unit 22 for storing the predetermined data. Herein, the predetermined data preferably includes a word per bank, a row per unit line, an offset, and a base row value. The base row denotes a start row address of one frame or one field.

A schematic construction of the memory access control apparatus according to the present invention to which a memory access control unit is applied will be explained with reference to Figure 7.

Figure 7 is a view showing a schematic flow for accessing the R, G, and B image data of Figure 6 to the memory.

As shown, the memory access control unit 20 temporarily stores R, G, and B image data format-converted in the format conversion unit 10 in each first in first

out (FIFO) and then multiplexes thus to store in the external memory at one time. Then, the memory access control unit 20 reverse-multiplexes the R, G, and B image data stored in the external memory thus to store in said each FIFO memory, and then outputs to the format conversion unit 10.

In case that the R, G, and B image data are accessed as respective R, G, and B image data, a memory access latency is substantially increased to three times than a case that the R, G, and B image data are accessed as one unit, thereby degrading an efficiency of the entire system. That is, when a memory access latency necessary to access the image data at one time supposed to be 10, a memory access latency necessary to access the R, G, and B image data as one unit is 10 but a memory access latency necessary to respectively access the R, G, and B data is 30.

As aforementioned, in the memory access control apparatus according to the present invention, values of the row, the bank, and the column inside the memory where the image data is to be stored are calculated on the basis of coordinate values of the image data constituting one frame and predetermined data in order to realize the warping function such as a pin cushion or a keystone, thereby optimally controlling the memory access latency for various display apparatuses.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds

of the claims, or equivalence of such metes and bounds are therefore intended to be embraced by the appended claims.